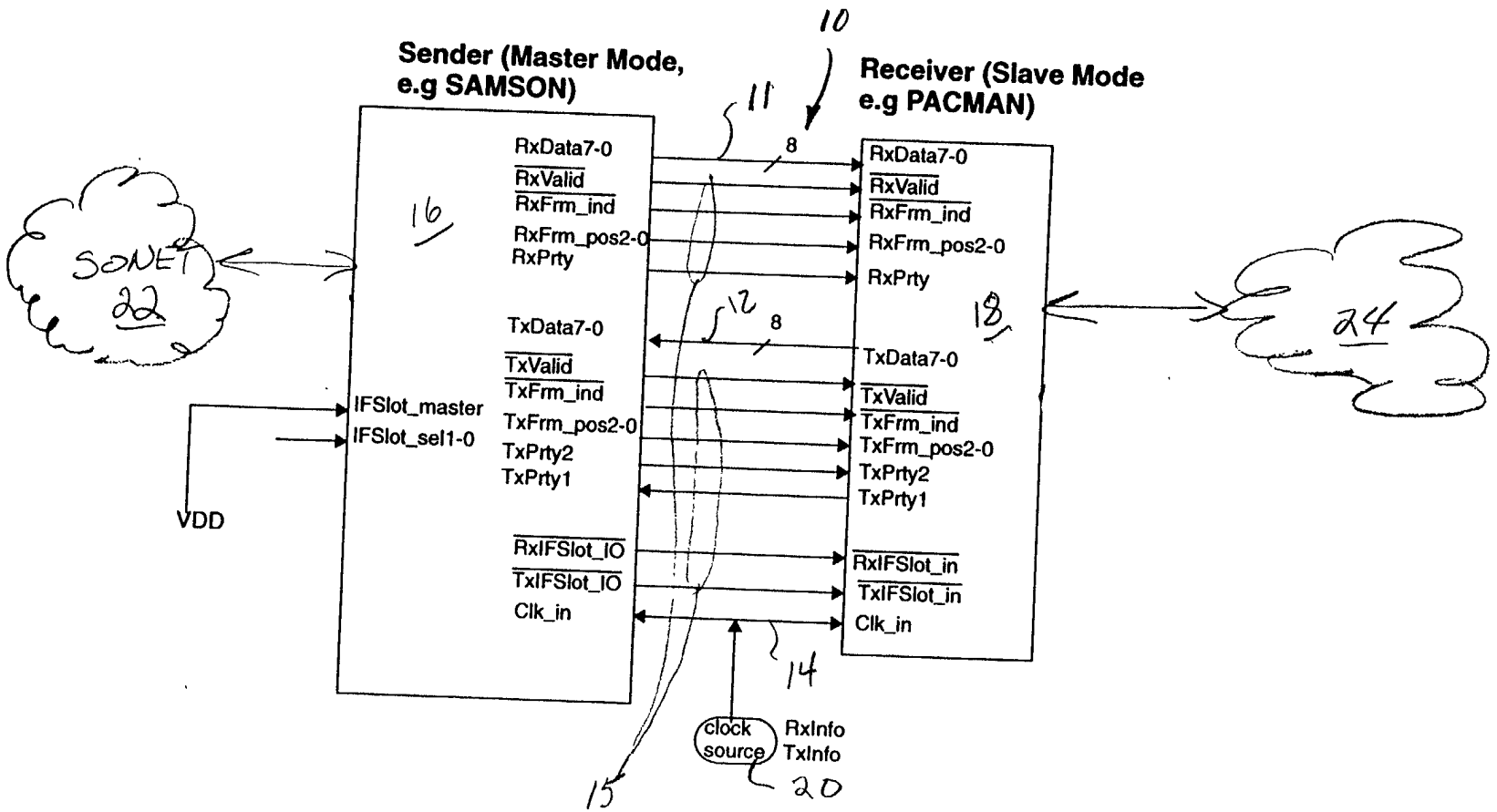

FIG. 1

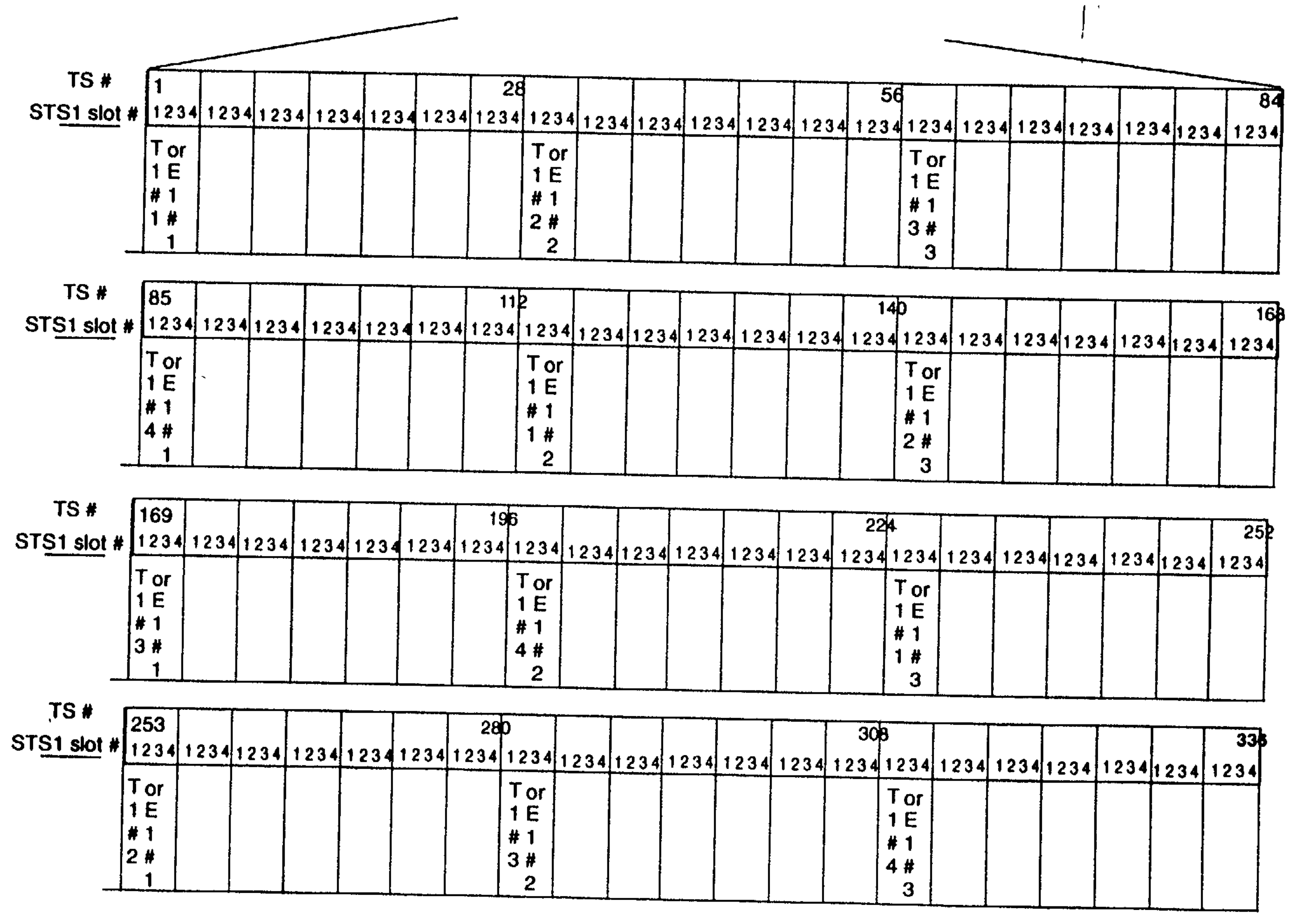
TS #
STS1 slot #
1
28
56
84
85
112
140
168
169
196
224
252
253
280
308
336
1 2 3 4
T or 1 E # 1 1 # 1
T or 1 E # 1 2 # 2
T or 1 E # 1 3 # 3
T or 1 E # 1 4 # 1
T or 1 E # 1 1 # 2
T or 1 E # 1 2 # 3
T or 1 E # 1 3 # 1
T or 1 E # 1 4 # 2
T or 1 E # 1 1 # 3
T or 1 E # 1 2 # 1
T or 1 E # 1 3 # 2
T or 1 E # 1 4 # 3

FIG. 2

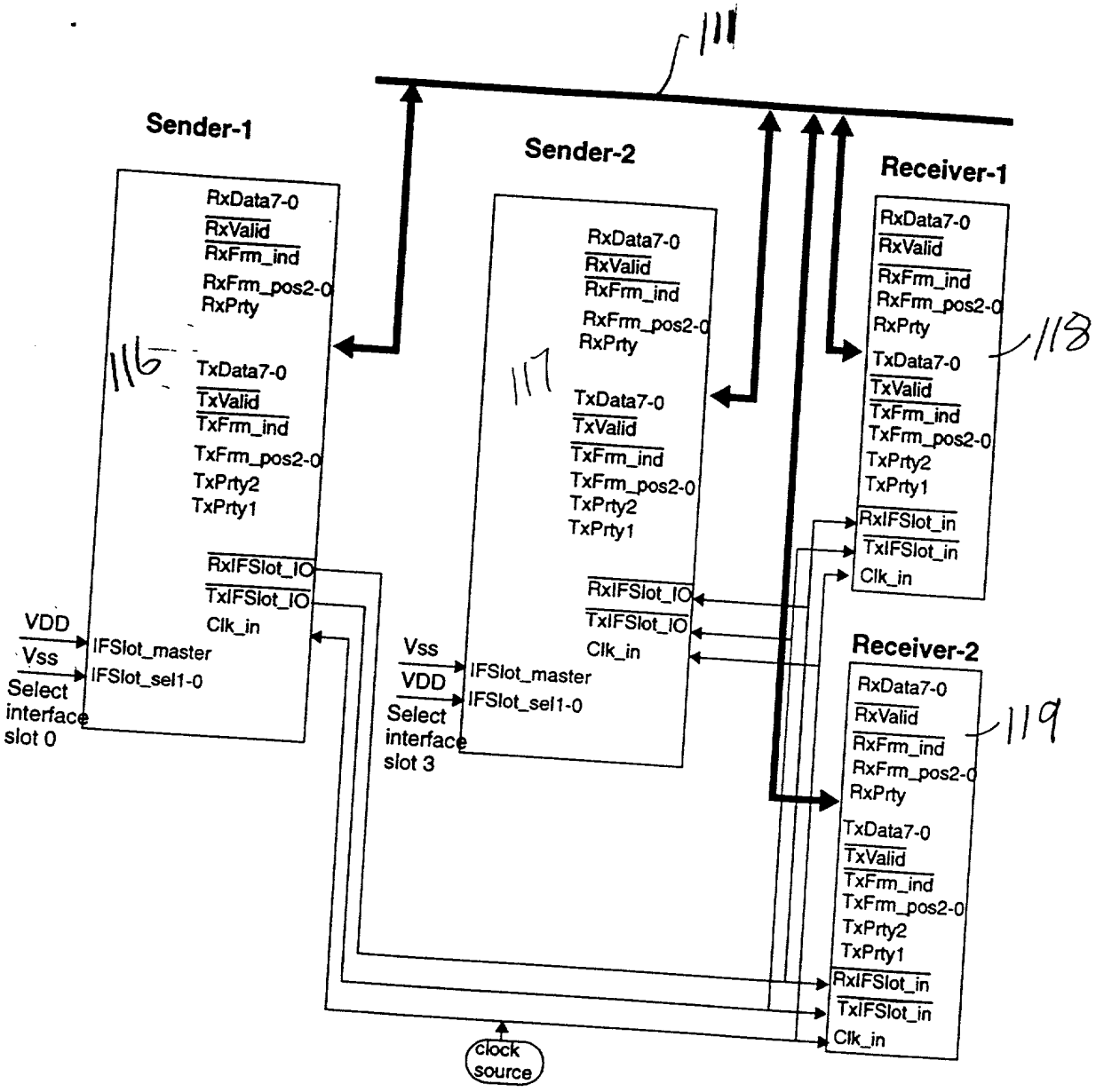
111
Sender-1
Sender-2
Receiver-1
Receiver-2
RxData7-0
RxValid
RxFrm_ind
RxFrm_pos2-0
RxPrty
TxData7-0
TxValid
TxFrm_ind
TxFrm_pos2-0
TxPrty2
TxPrty1
RxIFSlot_IO
TxIFSlot_IO
Clk_in
RxIFSlot_in
TxIFSlot_in
VDD
Vss
IFSlot_master
IFSlot_sel1-0
Select interface slot 0
Select interface slot 3
116
117
118
119
clock source

FIG. 3